13B IORQGE connects to the IORQ input of the ULA chip. It is also connected to the IORQ output from the Z80A via R27 (680R). If IORQGE is connected to +5 volts the ULA chip will not receive its IORQ signal from the Z80A. This could be useful for expanding the number of devices available for user I/O, A7 could be used to disable the IORQGE signal when it is low. You would then be able to use A0 — A6 in any combination to address any one of 128 I/O devices. A circuit to do this together with an experiment using IORQGE is given in chapter 14.

14B 0v another zero volts connection intended for use in conjunction with the video signals.

15B VIDEO
16 B Y
17B V
18B U

Video signals from the Spectrum. They are not normally connected up to their designated signals. You will have to do this yourself if you wish to use these outputs. VIDEO could be used to operate a monitor.

19B BUSRQ connected to the Z80A bus request input and held high by R30 (1K) to +5 volts. This can be used by external devices to request the use of all the CPU buses. Control is handed over after the current machine cycle is completed. The Z80A signals to the external device when its buses are available by taking BUSACK low.

20B RESET connected to the Z80A reset pin. This line is provided with a simple RC delay, at power on, to allow the whole computer to reach an operational state before the CPU tries to do anything. A simple RESET button can be connected between this pin and 0 volts (see fig 10b). When this switch is operated the CPU will reset in the same way as at power on. The difference is that you do not have to disconnect the power supply and then reconnect it. A RESET switch would be extremely useful to anyone who replaces the BASIC ROM with a machine code monitor, because memory would not then be erased whenever a reset had to be performed.

21B A7 address bus
22B A6 address bus
23B A5 address bus
24B A4 address bus

25B ROMCS connects directly to the ROM chip select pin and via R33 (680R) to the ULA. If you connect ROMCS to +5 volts the 16K BASIC ROM will disappear from the Spectrum memory. Obviously you must replace this with another program in some external memory at switch over, otherwise the computer will crash!

26B BUSACK the Z80A bus acknowledge signal tells an external device that it now has full control of the Z80A buses. It is used in conjunction with the BUSRQ signal.

27B A9 address bus
28B A11 address bus

CPU C register appears on A0 — A7 and the CPU B register appears on A8 — A15. From BASIC, a full 16 bit I/O address can be specified. This appears on A0 — A15 when IORQ is active.

18A RD the Z80A read output indicates that the CPU wishes to read data from memory or an I/O device. The addressed device should use this signal to put the relevant data onto the data bus.

19A WR the Z80A write output indicates that the CPU data bus holds data to be stored at the addressed location.

20A −5 volts power supply line. See the power supply circuit for details.

21A WAIT connected to the Z80A wait input, held high via R29 (1K5) to + 5 volts — this input can be used by slow external devices to make the CPU wait until they are ready to transfer their data. Care should be taken not to operate this line for long periods of time (ie more than 1ms) because dynamic memory will not be refreshed during wait states. The program or data could be corrupted and lost if WAIT is used for too long.

22A +12 volt power supply output (see power supply circuit for more details).

23A +12 volts NOT minus 12 volts as labelled in the Spectrum manual! This pin is in fact connected to the collector of TR 4 and is therefore an unsmoothed +12 volt supply. You should not use this as a +12 volt supply directly. The +12 volt supply from 22A should normally be used. A circuit to convert it to −12 volts is given in chapter 3.

24A M1 from the Z80A machine cycle one output — indicates that the CPU is currently getting the opcode for the next instruction to be executed from memory.

25A RFSH memory refresh signal from the Z80A. During a memory refresh the CPU R register appears on A0 — A7 and the CPU I register appears on A8 — A15. This can have interesting consequences if I has a value between 64 and 127. See chapter 8 for full details.

26A A8 address bus
27A A10 address bus
28A no connection.

SIDE B CONNECTIONS

1B A14 address bus
2B A12 address bus
3B +5 volts logic chip supply
4B +9 volts unregulated DC supply from the mains adaptor.
5B slot for locating the edge connector in the correct position.
6B 0 volts connection for the power supplies. Two connections are supplied because this line carries the sum of the other
7B 0 volts power supply currents. You should connect both to your external circuit to prevent either connection being overloaded.

8B CLK the 3.5 MHz clock signal from the ULA. Can be used to synchronise the operation of several Z80A support chips with the Z80A CPU. Note that the ULA may stop this clock for an odd cycle now and again if the CPU is accessing the first 16K of RAM. See chapter 8 for more details.

9B A0 address bus
10B A1 address bus
11B A2 address bus
12B A3 address bus