12. THE EDGE CONNECTOR

This chapter contains a contact by contact description of the signals available on the rear edge connector. Some hints and ideas to help you design your own circuits are included as well. For some simple experiments which you can do see chapter 14.

The connections designated 28A and 1A are marked on the upper side of the Spectrum board. 28B is under 28A and 1B is under 1A. Fig 10a illustrates the rear view of the Spectrum showing the correct orientation of the edge connector. Note that it is shown upside down in the BASIC manual!

SIDE A CONNECTIONS

1A A15 of the address bus. This can be used as an output from the Spectrum to select various external devices in conjunction with the rest of the address bus. It can also be used as an input to the Spectrum from any external devices which take over control of the CPU buses using the BUSREQ signal.

2A A13 of the address bus

3A D7 of the data bus. This bidirectional 8 bit bus can be used to transfer information to or from the Spectrum.

4A no connection

5A slot to locate the edge connector in the correct position.

6A D0 data bus

7A D1 data bus

8A D2 data bus

9A D6 data bus

10A D5 data bus

11A D3 data bus

12A D4 data bus

13A INT connected to the Z80A interrupt line, and via R26 (680R) to the ULA INT pin. This could be used by an external device to request an interrupt from the Spectrum, or if connected to +5 volts this will prevent the ULA from interrupting the Z80A CPU every 20 ms. See chapter 14 for an experiment using INT.

14A NMI to the Z80A non-maskable interrupt input. Normally held at logic 1 by R28(10K) connected to +5 volts. If taken low by an external device the Z80A will be forced to jump to address 102 decimal (66Hex) and start executing the machine code from there. See chapter 14 for an experiment using an NMI.

15A HALT from the CPU HALT output — indicates that the CPU has executed a software HALT instruction. The CPU waits for an interrupt from an external device before continuing to execute the program. See chapter 14 for a simple experiment using a HALT.

16A MREQ from the CPU memory request output — indicates that the address bus now holds a valid address for a memory read or write operation. This signal is also operated during a memory refresh.

17A IORQ connected directly to the Z80A input/ouput request output. Indicates that the lower half of the address bus holds a valid I/O address for an I/O operation. The upper half of the address bus holds the contents of the CPU A register if IN A,n or OUT n,A are used in a machine language program. n appears on the lower half of the address bus. If a register indirect I/O operation occurs, the

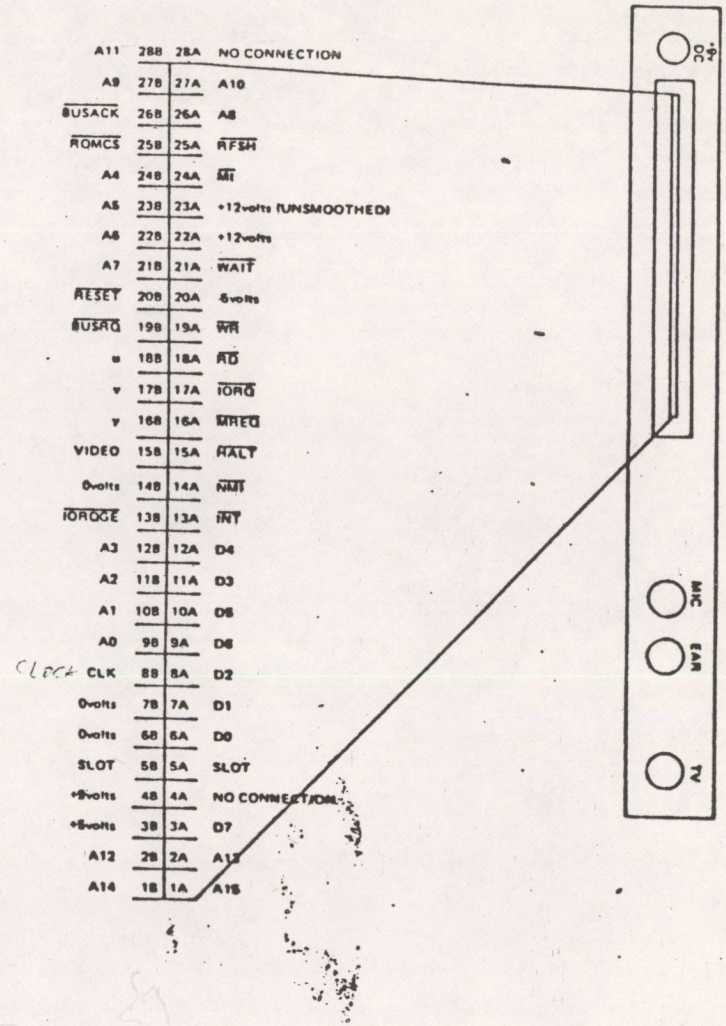

FIG 10a – THE EDGE CONNECTOR