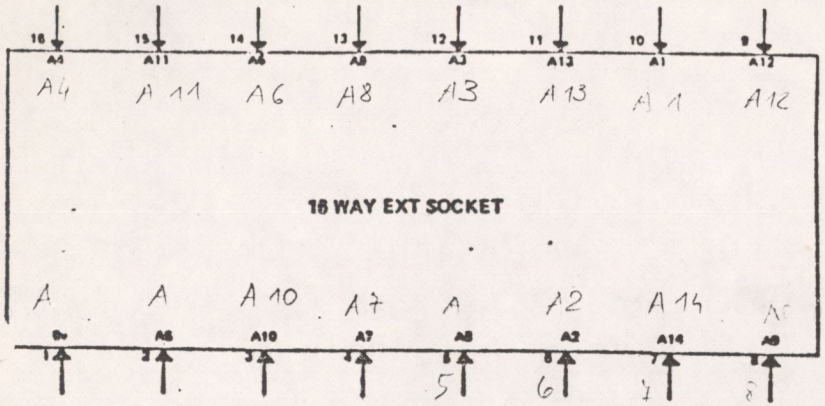

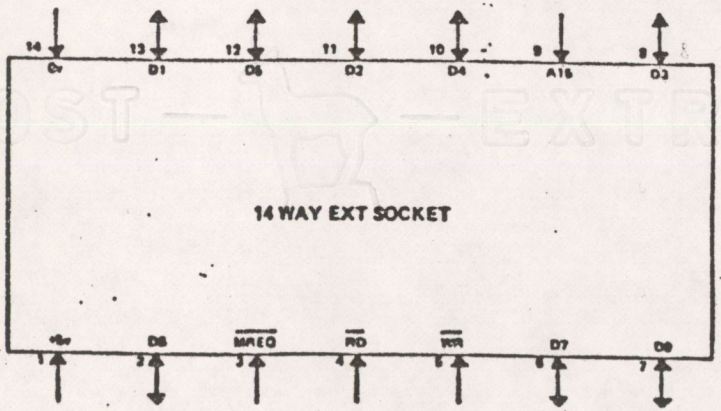

ISSUE 1 SPECTRUM

FIG 8a – MEMORY EXPANSION SOCKETS

3. Memory Refresh

When a refresh cycle is executed by the Z80A, $\overline{WR}$ and $\overline{RD}$ remain inactive in the logic 1 state. The address multiplexers are therefore set to direct A0-A7 to the memory array. The Z80A puts the number of the row to be refreshed on A0-A6 (7 bits allow 128 different row addresses). $\overline{MREQ}$ then goes low to operate the $\overline{RAS}$ line on the memories. This is all that is required for a refresh. Each of the 128 rows are refreshed at least once every two milliseconds by this method. Continual refreshing by the CPU was not required for the video memory except during field synchronisation pulses to the television. This is because the ULA is accessing the video memory sequentially at each of the 128 row addresses during video data output.