9. THE MEMORY EXPANSION SOCKETS

To upgrade an issue 1 16K Spectrum to a 48K Spectrum, the extra 32K of RAM can be plugged into the two sockets on the main board. Referring to fig. 8a, all address and data bus lines appear on these two sockets, together with essential memory control signals from the Z80A CPU.

These sockets are unlikely to be of use to any 48K Spectrum owners, since they are already being used. 16K Spectrum owners could use these sockets to add on their own 32K of RAM. Bear in mind that Sinclair has used eight 32K bit memory chips. These are actually 64K bit ones which don't work as 64K chips! If you use the more readily available 4116 16K bit memory chips then sixteen will be required. The original power supplies will almost certainly not be able to supply enough current for 16 chips, so you will need to add another power supply as well.

Note: Only the first 60 000 Spectrum computers (issue 1) will have these expansion sockets. New ones (issue 2) have sockets for all of the extra memory chips to plug directly into the main board. If you can find really cheap 64K chips, these can be used instead of Sinclair's 32K ones.

The memory expansion circuit diagram is illustrated in fig 8b. Its mode of operation is very similar to that of the 16k video RAM described in chapter 5. The major difference is that the row address strobe (RAS) and column address strobe (CAS) signals are generated by a selection of logic gates and not by the ULA. The circuit operates in one of three possible modes:

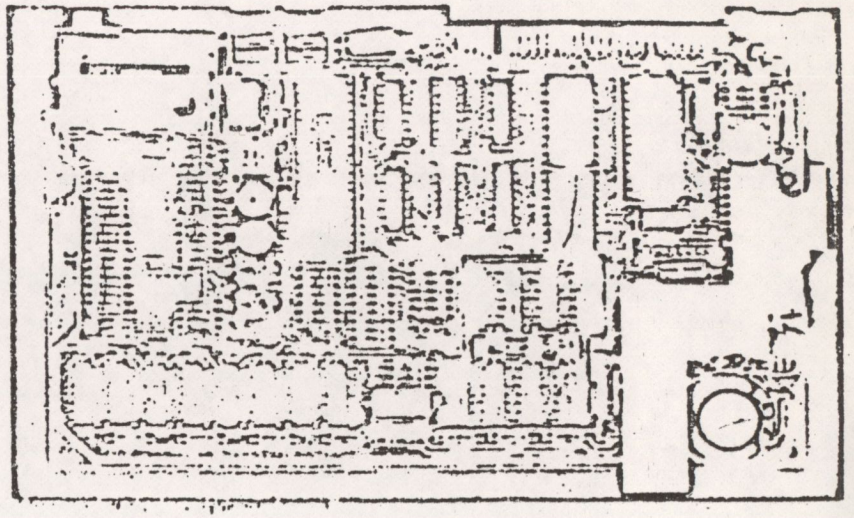
1. Memory Read

When the CPU wishes to read some data from this 32k block of memory, A15 will be at logic 1. RD and $\overline{\text{MREQ}}$ will then both be pulled low by the Z80A. The high to low transition of $\overline{\text{MREQ}}$ takes $\overline{\text{RAS}}$ low to latch A0-A7 into the eight dynamic RAM chips. The address multiplexers always direct A0-A7 to the memory chips whilst $\overline{\text{MREQ}}$ is high. The RC network comprising R2 and C2 delays the high to low $\overline{\text{MREQ}}$ transition from reaching the address multiplexers. This gives the memory chips a chance to latch A0-A7 before the multiplexers direct A8-A14 to the dynamic memories. The RC network comprising R1 and C1 then delays the signal again before operating $\overline{\text{CAS}}$. This allows the multiplexers time to switch over the address data. After the operation of $\overline{\text{CAS}}$, the full 15 bit address will have been latched into the dynamic memory chips. After a further short delay, the required data appears on the Spectrum data bus so that it can be read by the CPU.

2. Memory Write

When the CPU wishes to store some data in this extra 32k of memory, A15 is again set to logic 1, then $\overline{\text{WR}}$ and $\overline{\text{MREQ}}$ go low. The difference between writing and reading is that the WR pin on the dynamic memories is pulled low by WR but not by $\overline{\text{RD}}$. The memory chips therefore know that they must store data from the CPU data bus instead of outputting data.

ISSUE 2 BOARD



ISSUE 1 BOARD

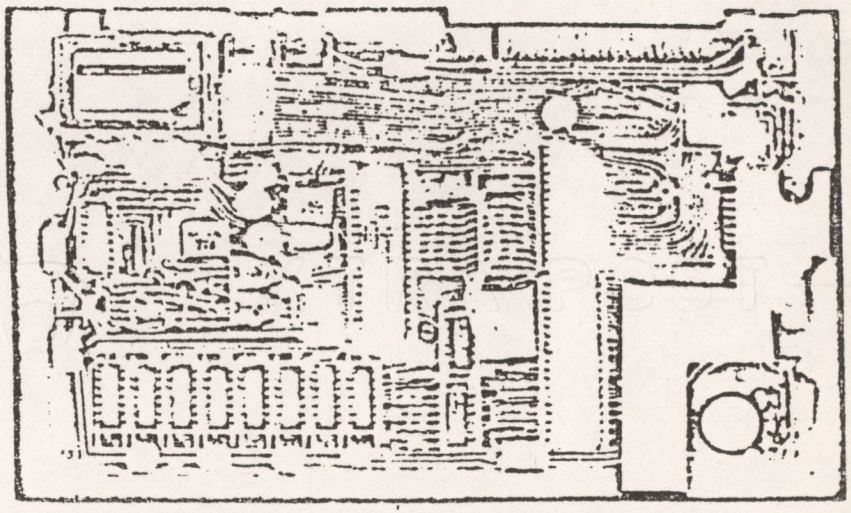


PLATE 8a – PHOTO OF MAIN SPECTRUM BOARD WITH MEMORY EXPANSION SOCKETS OUTLINED