5. VIDEO AND PROGRAM MEMORY

This 16K of RAM is supplied on both the 16K and 48K versions of the Spectrum. It contains all of the data for generating the display on the television screen, the various variables required by BASIC, workspace, user defined graphics and your BASIC programs.

Now refer to fig.4. Each of the memory chips IC7 — IC14 can store 2^{11} = 16K (K just means 1024) bits of information. Eight of them are required to make up the 8 bit data bus. So that the memories can fit into smaller chips with fewer connections, the address lines are multiplexed. This means that first of all A0 — A6 are presented to the memory chip, followed by A7 —A14. These two sets of 7 bits are latched within the memory chip. The memory chip is then able to select the correct location. IC3 and IC4 do this multiplexing, the selected address lines diverted to the memory chip inputs being determined by the state of the select pin 1 on IC3 and IC4. DRAM A0 — DRAM A6 on the ULA can override the outputs from IC3 and IC4 because of the 330 ohm resistors in series with the multiplexer outputs. This override capability enables the ULA to get data for output to the video circuit whenever it is required. You may now be wondering what would happen if the CPU and ULA both wanted to access this memory simultaneously. Obviously they cannot both access two different memory locations at the same time. The resolution of this conflict will be described in chapter 8 on the ULA.

The type of memory used here is called dynamic random access memory. The internal memory array is arranged as 128 rows by 128 columns of cells. The row address strobe (RAS) and column address strobe (CAS) signals are used to latch the relevant addresses into the memory chips. Data can then be written to or read from the addressed location. Each row must be accessed at least once every 2mS otherwise the memory may forget what is stored inside it. In the Spectrum this refreshing is not a problem whilst video output is occuring, because the video memory has to be regularly accessed to produce a continuous video display. During the video field sync, when the memory is not accessed for about 5mS, the normal CPU refresh takes over. Memory which can be read from and written to, but which does not require this continual refreshing procedure is called Static RAM. In both types of RAM, the data is lost when the power is disconnected.

FIG 4 – VIDEO AND PROGRAM RANDOM ACCESS MEMORY CIRCUIT DIAGRAM