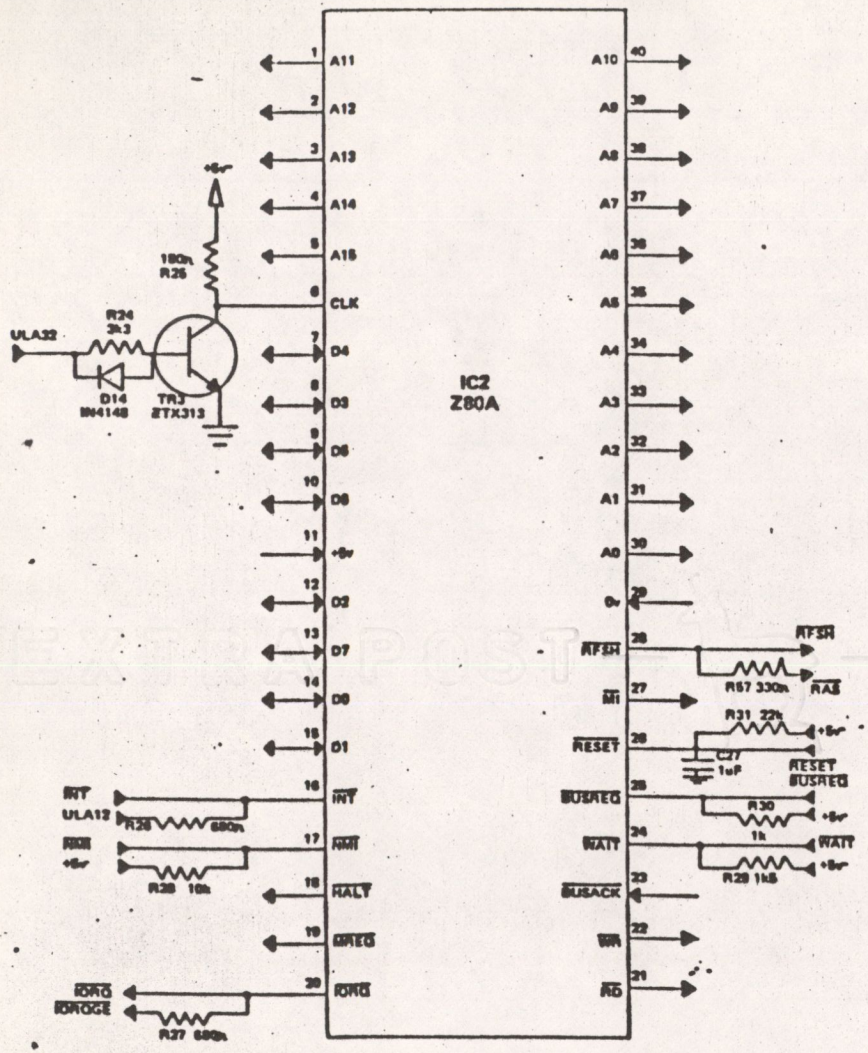

FIG 3 – Z80A CENTRAL PROCESSING CHIP

valid refresh addresses on the lower 7 bits of the address bus.

D0 — D7 The data bus — these eight tristate bidirectional lines are used for data input and output transfers with the CPU. Transfers take place between memory or peripheral devices and the Z80A.

$\overline{M1}$ Machine cycle one — Output active low. The signal means that the CPU is currently getting the Op-code for the next instruction to be executed from memory. $\overline{M1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

$\overline{MREQ}$ Memory request — tristate output, active low. This signal indicates to the memory that the address bus now contains a valid address for a read or write operation. This signal is required to distinguish between a memory or input/output operation. For example, $\overline{MREQ}$, $\overline{RD}$ and $\overline{ROMCS}$ must all be active before a read from the BASIC ROM can take place (see fig 5).

$\overline{IORQ}$ Input/output request — tristate output, active low. Indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. This signal is required to distinguish between an input/output or memory operation. Note that $\overline{IORQ}$ and $\overline{MREQ}$ will never be active at the same time.

$\overline{RD}$ Read — tristate output active low. Indicates that the CPU wishes to read from memory or an I/O device. The addressed device should use this signal to put the relevant data onto the CPU data bus.

$\overline{WR}$ Write — tristate output, active low. Indicates that the CPU data bus holds data to be stored at the addressed location, or output to the selected I/O port. Memory should use this signal to store the data from the data bus.

$\overline{RFSH}$ Refresh — output active low. Indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories. This is required by dynamic memory chips so that they do not forget. If they are not fully refreshed at least once every two milliseconds, there is a danger that memory will be lost. When this signal is present, the upper 8 address bus lines contain the CPU I register contents. This leads to a fault in the Spectrum hardware. By setting the I register to any value between 64 and 127, interesting contention for the video RAM occurs. A15 and A14 from the CPU are selecting the 16K of RAM which the ULA normally has priority over. In this case, although the relevant address occurs with $\overline{MREQ}$ active, no $\overline{RD}$ or $\overline{WR}$ signal occurs because it is a refresh. This combination of signals seems to confuse the ULA so that it doesn't stop the CPU clock properly. A BASIC program which will illustrate this problem is included in chapter 8 on the ULA.

$\overline{HALT}$ Output active low. Indicates that the CPU has executed a software HALT instruction. It awaits an interrupt from another device before it will continue operation. There is a simple experiment illustrating the operation of a HALT in chapter 14.

$\overline{WAIT}$ Input active low. Used by slow memory or I/O devices to tell the CPU that they are not yet ready for a data transfer. The CPU sits back doing nothing until the slow device indicates that it is now ready.

$\overline{INT}$ Interrupt request — input, active low. This signal can be generated by external devices to make the CPU run a special machine code program somewhere in memory. If the internal software controlled interrupt enable flip-flop is enabled, the CPU will accept and acknowledge the interrupt. A flip-flop is equivalent to one bit of memory. The CPU uses this bit of its internal memory to remember whether or not it should accept interrupts from other devices. For more details on the use of interrupts, you should refer to a specialised book on the Z80.